REMARKS

This paper is submitted in reply to the Office Action dated May 18, 2006, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 1-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,308,290 to Forlenza et al. The Examiner did indicate, however, that claims 2 and 9 were directed to patentable subject matter.

Applicants respectfully traverse the Examiner's rejections to the extent that they are maintained. Applicants have amended claim 1 and added new claims 19 and 20. Applicants respectfully submit that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

As an initial matter the Examiner will note that new claim 19 corresponds to claim 2 as originally filed, and new claim 20 corresponds to claim 9 as originally filed. Given that the Examiner has indicated that claims 2 and 9 are allowable over the prior art of record, Applicants respectfully request consideration and allowance of new claims 19 and 20.

Now turning to the Office Action, and in particular the rejection of claim 1, this claim has been amended to clarify that pattern sets are applied to a scan chain "using" an ABIST circuit. The claim as amended now recites a method of detecting a defect in a scan chain, which includes applying a plurality of pattern sets to a scan chain using an array built-in self-test (ABIST) circuit coupled to the scan chain, collecting, from the scan chain, scan out data generated as a result of the application of the plurality of pattern sets to the scan chain, and using the collected scan out data to identify a defective latch in the scan chain.

Claim 1 has been rejected as being obvious in view of Forlenza. The Examiner may note that Forlenza is assigned to the same assignee as the instant application, and indeed, the first listed inventor, Orazio P. Forlenza, is also listed as an inventor of the instant application.

Forlenza discloses what is referred to as a "look ahead" scan chain diagnostic method, which is used prior to manufacturing to identify broken or stuck-at scan chains using test patterns that are generated and ready ahead of chip testing. Forlenza represented an improvement over prior designs that required test patterns to be generated at a tester, which required substantially more time and resources to diagnose scan chain failures.

In Forlenza, scan latches are coupled to combinational logic to both supply inputs to the combinational logic and capture outputs of the combinational logic, as shown in Fig. 1. Of note, combinational logic, as understood in the art, generates a predetermined output in response to particular stimuli, and there is no disclosure in the reference of the combinational logic incorporating any memory storage.

In contrast, claim 1 as amended recites the step of "applying a plurality of pattern sets to a scan chain using an array built-in self-test (ABIST) circuit coupled to the scan chain." As is well known in the art, an ABIST circuit is more typically used to test memory arrays in a circuit by applying test patterns to those arrays to identify defective memory cells in such memory arrays. In this regard, the "combinational logic" to which the Forlenza scan chains are coupled is not analogous to an ABIST circuit. Furthermore, there is no suggestion in the reference that the combinational logic could incorporate, or be modified to incorporate, ABIST circuitry that generates pattern sets for application to a scan chain.

Forlenza does disclose Built In Self Test (BIST) circuitry, e.g., at col. 5, lines 24-36. However, it is important to note that BIST is not specifically ABIST, as BIST circuitry can include a wide variety of types of test circuitry other than ABIST, e.g., Logical BIST (LBIST) circuitry. In the case of Forlenza, the BIST circuitry that is disclosed is separate from the combinational logic, and furthermore, is specifically used to store test patterns on-chip for the purpose of eliminating the need to load test patterns from off-chip when performing look ahead scan chain diagnostics. There is no disclosure or suggestion in the reference that the BIST circuit could specifically be implemented as ABIST circuitry, and indeed, given that ABIST circuits typically do not include any form of integrated memory storage, Applicants submit that one of ordinary skill in the art

would not be motivated by Forlenza to utilize ABIST circuitry to perform the functions allocated to the BIST circuitry disclosed in Forlenza.

In fact, given that ABIST circuits *generate* test patterns, rather than retrieve test patterns from any form of memory storage, Applicants respectfully submit that Forlenza, and in particular, the disclosure of BIST circuitry that incorporates memory storage for storing test patterns, specifically teaches away from the use of an ABIST circuit to generate pattern sets, as recited in claim 1.

The Examiner acknowledges that Forlenza does not specifically disclose an ABIST circuit, but instead asserts that ABIST is merely a "design choice" (Office Action, page 4, lines 6-8). Applicants, however, respectfully submit that the use of an ABIST circuit, as recited in claim 1, is more than a mere design choice, as it is the ABIST circuit that generates pattern sets, and thus eliminates the need to store test patterns on chip as is required using the BIST circuit in Forlenza. Indeed, given that modern chip designs may incorporate tens of thousands (or more) of scan latches, the storage requirements required to store test patterns suitable for testing each of the scan latches in a design can be substantial. The use of an ABIST circuit eliminates the need to store a large set of test patterns on a chip, and as such, represents a unique and unexpected advantage over the prior art of record.

Applicants therefore respectfully submit that claim 1 is non-obvious over Forlenza and the other prior art of record. Reconsideration and allowance of claim 1, and of claims 2-7 which depend therefrom, are therefore respectfully requested.

Next, with respect to independent claims 8 and 17, each of these claims recites, in part, the concept of "collecting, from [a] scan chain, scan out data generated as a result of an application of a plurality of pattern sets to the scan chain by an array built-in self-test (ABIST) circuit" for the purpose of identifying a defective latch in the scan chain. As discussed above in connection with claim 1, Forlenza does not disclose or suggest the concept of applying pattern sets to a scan chain using an ABIST circuit, and the use of an ABIST circuit to perform such a function represents more than merely a design choice. Accordingly, claims 8 and 17 are non-obvious over Forlenza for the same reasons

presented above for claim 1. Reconsideration and allowance of claims 8 and 17, and of claims 9-16 and 18 which depend therefrom, are therefore respectfully requested.

Next, with respect to the various rejected dependent claims, Applicants traverse the Examiner's rejections based upon the dependency of these claims on the aforementioned independent claims. A number of these claims, however, recite additional features that further distinguish these claims from the prior art of record, and warrant additional mention.

For example, claims 5 and 12 recite the concept of laterally inserting pattern sets into the scan chain using the ABIST circuit. As shown, for example, in Figs. 7A and 7C, and as described at page 6, 14 and 15, the use of an ABIST circuit to laterally insert pattern sets into a scan chain eliminates the need to load pattern sets through the scan input of the scan chain, given that a defective latch in a scan chain often prevents a test pattern from being properly loaded into any downstream latches. Applicants can find no disclosure or suggestion of this concept in Forlenza, and the passage relied upon by the Examiner, at col. 3, lines 9-31, merely lists various types of scan chain fails, and thus appears to be irrelevant to the concept of laterally inserting pattern sets into a scan chain.

In addition, claims 7 and 14 recite the concept of reconfiguring a scan chain prior to collecting the scan out data. The passage cited against these claims by the Examiner, at col. 4, lines 30-38, discloses only passing 0 and 1 patterns through a scan chain, and is completely silent with respect to reconfiguring a scan chain.

Accordingly, Applicants submit that the Examiner has failed to establish a *prima facie* case of obviousness as to claims 5, 7, 12 and 14. Reconsideration and allowance of these claims are therefore respectfully requested.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits

are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

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Date

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